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Monolithic radio frequency SiN_x self-rolled-up nanomembrane interdigital capacitor modeling and fabrication

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Abstract

Monolithic capacitors operating at radio frequencies (RF) serve as critical components in integrated circuits for wireless communication. Design and fabrication innovations for high capacitance density RF capacitors are highly desired for the miniaturization of RFIC chips. However, practical and simple solutions are limited by existing capabilities in three-dimensional (3D) structure construction and the effective configuration of electrodes. We report a unique route to achieve unprecedentedly high capacitance density at a high operating frequency through a capacitor configuration of 3D coil interdigital electrodes using planar semiconductor processing compatible materials and fabrication methods. A systematic mechanical-electrical design principle is demonstrated, and fabricated devices show a maximum 21.5 pF capacitance, which is 17.2× larger after rolling up. The corresponding capacitance density is as large as 371 pF mm^{-2}, with resonant frequency of 1.5 GHz. The performance could be improved significantly by simply rolling up more turns with minimal change to the area footprint.

Supplementary material for this article is available online

Keywords: interdigital capacitor, radio frequency, self-rolled-up nanomembrane

(Some figures may appear in colour only in the online journal)

1. Introduction

Controlled formation of three-dimensional (3D) self-rolled-up membrane (S-RuM) microtubes as a novel platform for functional devices is a topic of broad and increasing interest, particularly in the last decade. Uses of such microtubular architectures have been envisioned in nearly every aspect of practical applications, including photonics, metamaterials, biomedical devices, energy storage and electronics [1–12]. Since the first fabricated InAs/GaAs rolled-up tubes by Prinz *et al* [13], S-RuM tubes, made from a variety of strained materials have been demonstrated [14–18]. Among them, plasma enhanced chemical vapor deposition (PECVD) SiN_x multilayer microtubes are investigated particularly due to their compatibility with silicon integrated circuit fabrication processes (ICs), visible spectrum transparency, and non-toxicity to biological systems. The most popular SiN_x based S-RuM platform is designed with bilayer construction, which includes two 20 nm layers of oppositely strained thin film SiN_x deposited in sequence under different frequencies and other deposition parameters such as power, precursor flow

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ratios, in a silane (SiH_4)/nitrogen (N_2)/ammonia (NH_3) PECVD environment. With maximum stress optimization, SiN_x thin film deposited under high frequency (HF) at 13.56 MHz or low frequency (LF) at 380 kHz obtains tensile or compressive stress of 406.95 MPa or −1168 MPa, respectively. The self-rolling procedure is then triggered by directionally releasing the SiN_x thin film bilayer from the sacrificial layer. Such a combination of LF and HF SiN_x bilayer covered by an atomic layer deposition (ALD) Al_2O_3 thin film for lateral etch guidance and reduction of rolling issues caused by PECVD SiN_x pin holes has been proven as a potential pathway for the miniaturization of monolithic radio frequency (RF) devices [4, 19–22]. With the guidance of precision quasi-dynamic mechanical and electromagnetic (EM) FEM modeling [23, 24], SiN_x S-RuM inductors and transformers have been successfully demonstrated with exceptional electrical performance, competitive size, and high fabrication yield.

However, on the road map towards all-S-RuM-passive-device-based compact RFICs, qualified S-RuM capacitors for IC layout construction have been missing due to both design and fabrication issues. Effort has been made using a hybrid dielectric layer consisting of HfO_2 and TiO_2 incorporated into an Al_2O_3 matrix to obtain ultracompact capacitors for electrostatic energy storage [25, 26]. However, the metal-insulator-metal (MIM) capacitor structure was found out not suitable for HF operation, and the capacitance saturates when the number of turns is over two. Mechanical considerations also set practical constraints on the layout design and therefore the overall electrical performance of these MIM capacitors.

In this paper, we reported a systematic study of the interdigital layout for realizing S-RuM RF capacitors and the design principles associated with such devices. The proposed processing flow obtains high fabrication yield. The measured performance of fabricated devices matches very well with the expected simulation results, which demonstrates the effectiveness of the design principle.

2. Structural design

Figure 1 shows the step-by-step monolithic process flow used for the fabrication of S-RuM capacitor on a sapphire substrate which is the same as that in [19]. As a commonly used, highly conductive metal in RFIC processing, Cu with a thickness of up to 180 nm is chosen as the conductive material in this study. Thicker Cu could be used if the introduced rolling resistance is not a barrier to desired rolling results. Figures 1(a) to (b) show the processing steps to form a mesa containing the germanium (Ge) sacrificial layer and the SiN_x strained bilayer on top. Generally, a sacrificial layer with a relatively large Young's Modulus is necessary to avoid relaxing strained energy from the SiN_x bilayer. In addition, the smooth surface of a Ge sacrificial layer effectively prevents reduced conductivity of the Cu conduction layer from surface roughness scattering. The SiN_x bilayer is formed by

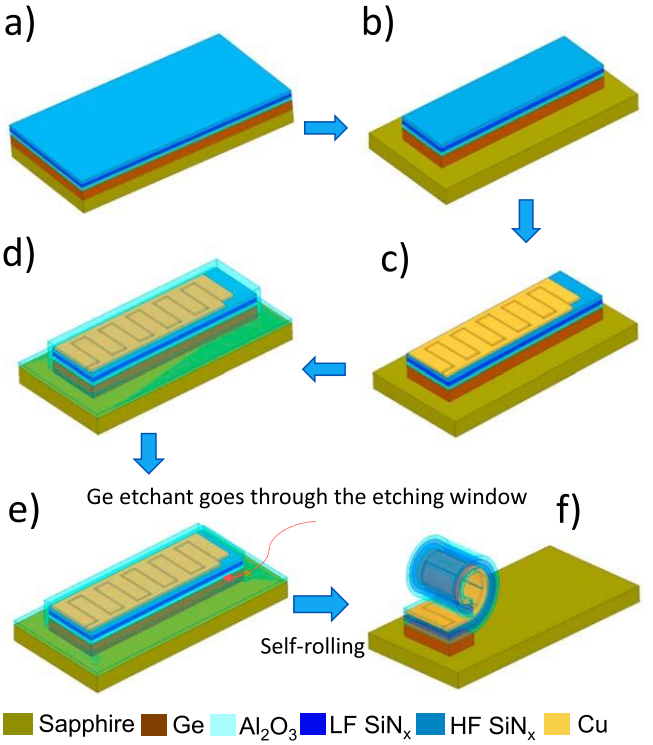

Figure 1. Schematic illustration of the 3D S-RUM interdigital capacitor fabrication processing flow. (a) Deposition of Ge, Al_2O_3, low-frequency (LF) SiN_x and high frequency (HF) SiN_x layers in sequence on a sapphire. (b) First lithography step to define a mesa by RIE. (c) Metal layer deposition by electron-beam evaporation and second lithography step to define the metal pattern. (d) Al_2O_3 cover layer deposition by ALD. (e) Third lithography step to define an etching window. (f) Removal of Ge sacrificial layer to trigger the self-rolling process of the stacked membrane. All materials are color-coded as indicated in the color bar.

depositing the LF SiN_x and HF SiN_x in sequence by PECVD. The compressive and tensile stresses are therefore embedded in the LF SiN_x and HF SiN_x thin film, respectively, and are maximized to provide a sufficient rolling force to roll up the Cu and Al_2O_3 cover layer.

For best results, a 5 nm Nickel (Ni) thin film is deposited as an adhesion layer between the Cu layer and the HF SiN_x layer. In demonstration, the thickness of Cu layer is 180 nm and is patterned by the second lithography step to form the layout of interdigital electrodes as shown in figure 1(c). Thereafter, a 20 nm Al_2O_3 thin film, deposited by ALD, is used to conformally cover the Ge/SiN_x mesa in order to guide rolling and to reduce the fabrication failure due to pinhole issues. The last lithography step and dry etch open an etching window on the opposite end of the mesa to the contacts. The window cuts through the Al_2O_3 cover layer and etches the end of the mesa itself to provide a uniform lateral etch front as shown in figure 1(e). Figure 1(f) shows the rolled-up architecture after the Ge etchant releases the sacrificial layer completely. Compared to traditional planar semiconductor processing, it can be found that, by utilizing strain differences among layers, the same 2D processing techniques is able to obtain 3D hollow cylindrical geometry above the substrate.

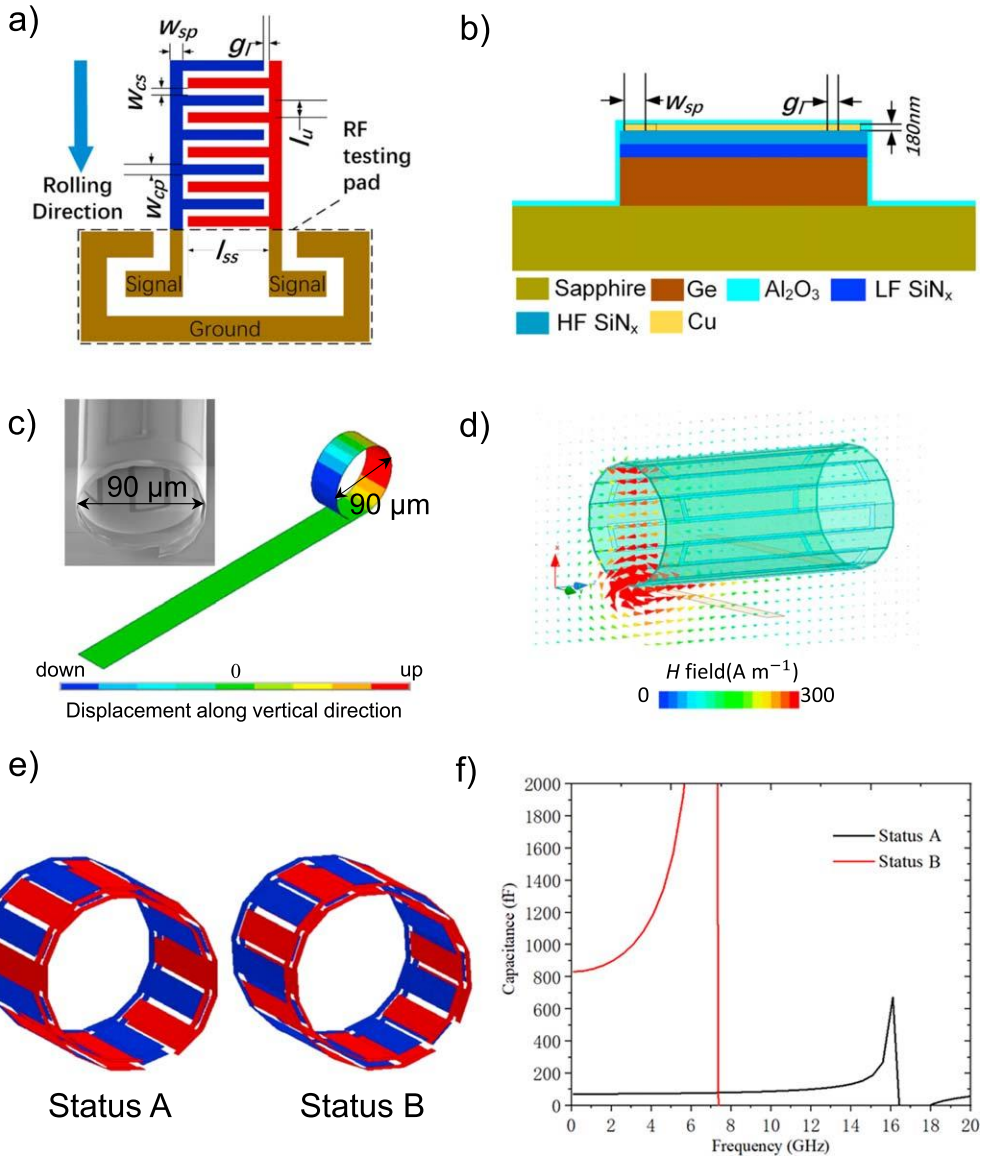

Figure 2. S-RUM capacitor design rationale. (a) The horizontal layout of S-RUM capacitor with dimensional parameters labeled. (b) The vertical membrane structure of S-RUM capacitor with key dimensional parameters labeled. (c) Comparison of measured inner diameter from the SEM image and the simulated structure. (d) Electromagnetic FEM model with simulated H field distribution plotted at 17 GHz on the cross-sectional x–z plane. (e) Two extreme cases of the overlapping configuration of adjacent electrodes. (f) The simulated capacitance versus frequency of the two extreme cases status A and B.

3. Electrical design

The general design principles could follow the flow for the design of S-RuM RF transformers [19]. Both of the structural dimension of the horizontal layout and the vertical membrane, shown in figures 2(a) and (b), respectively, need to be involved in the electrical design for desired performance. The electrical energy is capacitively stored in between the interdigital electrodes which are colored blue and red shown in figure 2(a). Assessment of the inner diameter serves as a fundamental consideration for the horizontal layout design, which could be done by mechanical modeling using quasi-static FEM (see details in methods 5.1). Figure 2(c) shows excellent matching between the simulated inner diameter and the measured data by SEM of a S-RuM interdigital capacitor sample. The horizontal layout design follows the conventional design rule of the planar interdigital capacitor. In general, the capacitance increases as the gaps g_l and w_{cs} between the two electrodes are decrease, and the smallest repeatable gap is determined by lithography resolution. Even for calculating the LF capacitance, analytical methods could quickly become convoluted. When the width of the finger w_{cp} equals the gaps g_l and w_{cs}, an analytical expression shown below is reported to estimate the value of the capacitance C_p per unit length [27]

$$Cp = \left(\frac{\varepsilon_r + 1}{w}\right) l_{ss}[(N-3)A_1 + A_2]\ \text{pF/unit length}, \quad (1)$$

where N is the number of fingers, w is the base width of the interdigital capacitor, l_{ss} is the length of the fingers, ε_r is the relative dielectric constant of the substrate, and the value of A_1

Table 1. Geometrical details of S-RuM interdigital capacitor samples.

Symbol	w_{cp}	w_{cs}	w_{sp}	g_l	l_{ss}	l_u	*# of fingers*	*Footprint*
Type A	10 μm	5 μm	5 μm	5 μm	205 μm	30 μm	12	245×90 μm^2
Type B	20 μm	5 μm	20 μm	5 μm	200 μm	50 μm	23	445×90 μm^2
Type C	5 μm	5 μm	20 μm	5 μm	200 μm	50 μm	23	645×90 μm^2

and A_2 depends on the ratio of T/g_l (T is the thickness of the substrate). After rolling up the planar interdigital layout, the analytical calculation of the rolled-up capacitance C_r could be even more complicated. By observing equation (1), the value of a device's capacitance will vary significantly after becoming rolled-up, due to the change of ε_r, A_1 and A_2, when the interdigital electrodes are away from the original substrate. For more accurate analysis, EM FEM modeling is used to investigate the value of the rolled-up capacitance C_r and its dependence on operating frequency.

Figure 2(d) shows the EM models of S-RuM interdigital capacitor with one turn before and after being rolled up, which are built in the high frequency structure simulator (see details in methods 5.2). The magnetic field strength is plotted on the cross-section plane of the tubular structure, which shows relatively strong magnetic flux through the ends of the structure, indicating that parasitic inductance is introduced by rolling up the electrode feedlines. One turn rolling does not fully utilize the controlled formation of tubular architectures to increase the capacitance density. The multiple-turn rolled-up device capacitances C_r depend on the inner diameter D, which can be further classified into three major different working statuses, and the two extreme cases are shown in figure 2(e). If the width of the electrodes is the same and as the gaps, the basic unit of the periodical interdigital layout is l_u, as shown in figure 2(a). The increment of the inner diameter is reasonably negligible as the inner diameter is usually larger than 90 μm, the value of the circumference of each turn divided by the unit length of l_u could be an even number or an odd number or a non-integer number. An even quotient means the overlapping electrodes on adjacent turns have the same polarity (status A), while an odd quotient means the opposite case (status B). Except for the two extreme status, non-integer quotient (status C) implies the performance of the S-RuM capacitor is in between that of status A and B. Figure 2(f) shows the EM simulation results of the two extreme working statuses, which clearly shows that overlapping opposite polarity electrodes on adjacent turns (status B), with a $>10\times$ larger capacitance compared to status A, is the desired design to fully utilize the S-RuM platform for high density capacitance HF capacitors. To understand the total capacitance dependence on diameter, we first analyze the dominant sources of capacitance present in the device: (1) the capacitance generated by fields normal to the metal layer between turns, (2) fringing fields capacitively couple fingers that are not directly parallel and overlapping, but adjacent in either the same or different turns. For traditional planar capacitors, these fringing capacitances are the dominant mode of capacitance, whereas for rolled-up capacitors, these capacitances contribute on top of the overlapping fingers from turn to turn. If all finger dimensions are held constant and a smaller diameter does not change the working status of S-RuM interdigital capacitor, the total capacitance is nearly independent on the diameter variation. However, if the diameter change is large enough to switch the working status of S-RuM interdigital capacitor among Type A, B and C, the total capacitance will be strongly dependent on the diameter variation, which is good in some cases when capacitance reconfiguration is desired. Qualitatively speaking, there is an upper limit of capacitance enhancement of status B electrode configuration which depends on the even number of the circumference of each turn divided by the unit length of l_u, or the value of the inner diameter. The larger the even number (the smaller the diameter to obtain even number), the closer the enhancement of capacitance is to its limit.

4. Fabrication and measurement results

Following the mechanical and electrical design approach, a diverse set of S-RuM monolithic capacitor structures are fabricated and measured with geometric-details shown in table 1. Figure 3(a) shows a set of photo images of S-RuM capacitors before and after rolling up with designs. The ability to realize excellent fabrication yield of the proposed structural design with the given processing method is also demonstrated. The corresponding electrical performance of capacitance versus frequency of S-RuM capacitors before and after rolling up are extracted from the measured S-parameters and shown in figure 3(b), which perfectly match the prediction from the EM modeling (figure 2(f)). The type A device shows decreased capacitance after rolling up, meaning the working status tends towards status A configuration of electrodes dominates the electrical performance. The type B and C devices both show significant enhancement of capacitance. The capacitance of the type C device specifically improves from 1.25 to 21.5 pF by rolling with a corresponding capacitance density as large as 371 pF mm^{-2}. There is room for both type B and C devices to be pushed towards the extreme case of status B for larger capacitance. The quality factor of S-RuM interdigital capacitor is derived directly from the de-embedded raw Y-parameters based on the definition of quality factor, which can be represented by the following equation:

$$Q = \left| \frac{\mathrm{im}(Y_{11})}{Re(Y_{11})} \right|. \tag{2}$$

Because it is more reasonable to compare Q factor of capacitors with same capacitances, so figure 3(b) lower row only show the Q factor versus frequency of samples after rolling. Usually, leakage loss (R_p) is small and the $Q = (\omega CR)^{-1}$, where R is the equivalent series resistance of

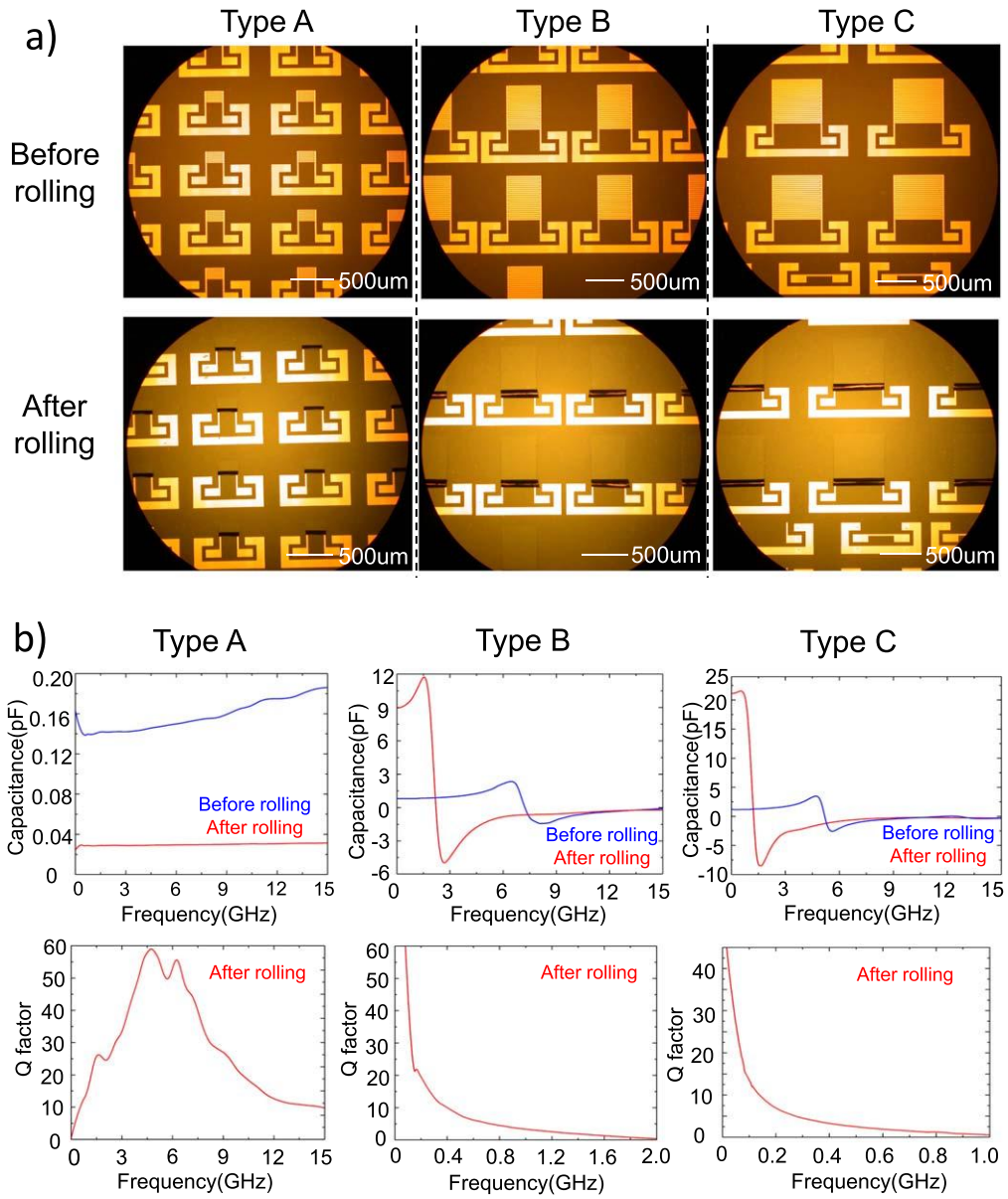

Figure 3. Photo images and performance of S-RUM capacitors. (a) A set of photo images showing S-RUM capacitors with different designs (Type A, B and C) before and after rolling. (b) Upper row: the measured capacitance versus frequency performance of the S-RUM capacitors with different designs (Type A, B and C) before and after rolling; lower row: the measured Q factor versus frequency performance of the S-RUM capacitors with different designs (Type A, B and C) after rolling.

Table 2. Performance comparison of rolled-up monolithic capacitors.

References	Structure	Capacitance	Resonant frequency	Footprint	Capacitance density
[25]	3D rolled-up	4.6 nF	<1 MHz	0.002 mm^2	2300 nF mm^{-2}
[26]	3D rolled-up	9 nF	1 MHz	0.008 mm^2	1125 nF mm^{-2}
This work	3D S-RUM	21.5 pF	1.5 GHz	0.058 mm^2	371 pF mm^{-2}

the capacitor. Therefore, the value of Q is inversely proportional to the capacitance C and the angular frequency ω, as shown in Type B and C samples. However, when a capacitor is lossy, i.e. there is large leakage current between the electrodes (equivalent to a parallel connected resistance R_p with capacitance C), then $Q = \omega C R_p$. The parasitic inductances formed by the rolled-up feedlines of the interdigital capacitor introduce resonant frequency, so the quality factor versus frequency has the relationship shown in Type A. Considering Type A S-RuM interdigital capacitor sample has smaller capacitance, the leakage current loss more easily dominates the electrical performance. Nonetheless, even though the Q factor of Type B and C is not as large as its conventional commercial products (usually >100), which is due to the

Table 3. Material properties set in FEM modeling simulation.

Sublayer	Residual stress (MPa)	Young's modulus (GPa)	Poisson coefficient	Thermal expansion coefficient (1/°C)	Temperature increment (°C)
LF SiN_x	−1133	210	0.28	2.75×10^{-6}	1450
HF SiN_x	+387	210	0.28	-9.61×10^{-7}	1450
Ni	+790	200	0.31	-1.9×10^{-6}	1450
Cu	+650	126	0.35	-9.85×10^{-7}	1450
ALD Al_2O_3	+400	180	0.24	-9.9×10^{-6}	1450

Note. Sign – and + for the residual stress denote compressive and tensile stresses, respectively.

relatively large resistance from the thin metal film electrodes (as was the case for the low Q factor in S-RuM inductors [20, 21]), the S-RuM interdigital capacitors demonstrated in this paper should still be sufficient for most applications, including RF broadcasting, walkie-talkie handling equipment, etc.

Table 2 compares the performance of published monolithic rolled-up capacitors with different electrodes configurations. The rolled-up parallel electrode capacitors easily obtain large capacitance and capacitance density, but their performance degrades at high frequencies due to the thin film dielectric issues. Their improvement of capacitance is also less than 2× after rolling up, which can be attributed to the nature of the electrical limitations of parallel electrode 3D coils. S-RuM interdigital capacitors are comparatively better candidate for HF operating points due to enlarged gap between electrodes, but to achieve capacitance and capacitance density as large as that of other rolled-up structures, more turns and high dielectric constant material filling the gaps between electrodes are required in addition to optimized design of all geometries based on the simulated inner diameter for status B working mode.

5. Methods

5.1. Quasi-static FEM mechanical modeling

As the electrical performance of the HF electronics and optics is extremely sensitive to the dimensional parameters, it is critical to precisely predict the diameter of the innermost tube. A transient quasi-static FEM modeling method according to [23] is used to determine the inner diameter of the rolled-up structure instead of using analytical methods.

The proposed FEM method assumes that all materials are isotropic and linearly elastic. A fixed boundary condition is applied to all nodes at the bottom of the LF SiN_x thin film to mimic the Ge sacrificial layer. According to Mindlin–Reissner shell theory, shell elements can be used to simulate multilayer structures with controlled precision. Depending on the design of the structure, different layer thicknesses and material properties can be assigned to the respective layers. For the S-RuM lumped element platform, the Young's modulus E of the PECVD LF SiN_x and HF SiN_x thin films was set to 210 GPa. The Poisson's coefficient of the bilayer was set to 0.28. For both LF SiN_x and HF SiN_x membrane, their residual stresses are modeled by the coefficient of thermal expansion in the FEM. For temperature increments, all nodes in the simulation have the same setup value. Different coefficients of thermal expansion were assigned to different layers for simulating compression and tensile stresses. The values of compression and tensile stress were measured by a FSM 500TC metrology tool. The exact value of the stress can be determined by applying an appropriate temperature increment. The thermal coefficient of LF SiN_x is taken from the literature; its temperature increment is determined to be 1450 °C to reach the measured value. When the temperature increment is fixed at 1450 °C, the thermal coefficients of other materials can be determined to achieve their respective measured residual stresses. Table 3 summarizes all the material properties used in the simulation for figure 2(c).

5.2. EM FEM electrical modeling

Ansys EMs Suite 19.0 was used to build the EM FEM models. The interdigital capacitor models before and after rolled up are shown in figures S1(a) and (b), respectively (available online at stacks.iop.org/NANO/30/364001/mmedia). To reduce the computation load, a polygonal cylinder is used to model the actual round structure. To fit the actual case, air gaps may be introduced in between adjacent turns in the model, which decreases the coupling capacitance between turns to deviate the resonant frequency. The skin effect must be taken into consideration when using 100's μm wide metal strips as the electrodes. In simulation, impedance boundary conditions with imported values of equivalent surface resistance at various frequencies were applied to the metal sheet to model the skin effect.

6. Conclusion

S-RuM monolithic RF interdigital capacitors are demonstrated in this work by systematically investigating the structural and electrical design principles. A three-step simple lithography processing flow is utilized for realizing a '3D from 2D' self-assembling automatic rolling processes. As indicated by EM modeling in this study, all horizontal and vertical dimensions need to be collectively considered in design to obtain the best working status, status B, which can fully utilize the freedom of a 3D configuration of interdigital electrodes for capacitance enhancement. With a maximum

operating frequency of 1.5 GHz, the maximum capacitance of S-RuM interdigital capacitor is 21.5 pF. By adding more turns, optimizing the working status, narrowing the electrodes gaps and filling the electrode gaps with high dielectric constant material, there is room to achieve capacitance within the range of nF and μF with extremely high capacitance density.

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